UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,243	12/11/2001	Renerus Antonius Van Den Heuvel	NL 000674	3083

24737 7590 10/03/2003

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,243	VAN DEN HEUVEL, RENERUS ANTONIUS	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121:

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The rejection is no longer based in the teachings of Fulford, Jr. et al. because the teachings of Fulford, Jr. et al. are accumulative of the teachings of Jin et al., wherein the first spacer (408) is formed of silicon nitride, which inherently can be selectively etched with respect to the gate oxide as noted by applicant on instant page 6, lines 24-29. Also, Jin et al. teach a method of forming MOSFET structures, which includes a gate oxide layer between the source and drain region and a gate transistor provided locally over the gate oxide layer.

2. Claims 1-8 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. (U.S. 6,350,665 B1) in view of Odake et al. (U.S. 6,030,869).

In reference to claims 1, 6 and 8, Jin et al. (Figs.3-4D) in a related method to form a MOSFET structure teach a semiconductor device containing a field effect transistor with a gate electrode (404) provided locally over a gate oxide layer, a source region (412-0) and a drain region (412-1), wherein the source region (424-0) and the drain region (424-1) are formed, in the semiconductor body (402), on both sides of the gate electrode (404) and a part (424-1) of the drain region (424-1) bordering the gate

electrode (404) is provided with a lower doping concentration, and wherein a silicon nitride spacer (408) is produced on both sides of the gate electrode (404), which can be selectively etched with respect to the gate oxide, characterized in that for the formation of the drain region (412-1) and the lowly doped part (421-4) thereof, the drain region (412-1) being formed at a distance from the gate electrode (404) that is larger than the width of the spacer (408) (column 7, line 46 – column 9, line 45).

Jin et al. fail to teach forming a gate oxide over the surface of the semiconductor body; and forming the source and drain regions with two additional mask in layers deposited on the surface of the semiconductor body. However, Odake et al. (Figs.2a-3a) in a related method to form source and drain regions in a semiconductor device teach forming a gate oxide (3) over a semiconductor body (1); and forming source and drain regions with two masking layers (8, 13) deposited on the surface of a semiconductor body (1) (column 6, line 61 – column 7, line 67). Therefore, it would have been obvious to combine the teachings of Odake et al. and Jin et al. to enable the formation of a gate oxide and source and drain regions as taught by Odake et al.

In reference to claims 2-5, Jin et al. and Odake et al. teach wherein for the formation of the lowly doped part of the drain region a first masking layer extending so far as to be on the gate electrode is produced on the side of the gate electrode of the source region to be formed on the surface of the semiconductor body, and a second masking layer extending from the gate electrode up to the drain region to be formed is produced on the surface of the semiconductor body (Odake et al., Figs.2c and 3a); wherein at the location of the source region and the drain region the gate oxide layer is

provided with an aperture and that at the location of said aperture the gate electrode, the source region and the drain region are provided with a metal layer, comprising a silicide (Jin et al., column 9, lines 25 – 35); wherein on the gate electrode an isolating layer is deposited, on which a shielding electrode is produced at the location of the gate electrode (Odake et al., column 6, line 61 – column 7, line 5).

The combined teachings of Jin et al. and Odake et al. fail to teach converting the metal layer into a silicide layer with the aid of the underlying silicon and wherein the distance from the drain region to the gate electrode is chosen between 1 and 4μm. However, the examiner takes official notice that the process of converting a metal layer into a silicide layer is common practice within the scope of one of ordinary skill in the art and therefore it would have been obvious to use the underlying silicon layer to convert a metal layer to a metal silicide layer. Also, the examiner takes official notice that the dimensional range of the drain region to the gate region involves routine optimization within the scope of one of ordinary skill in the art. One of ordinary skill in the art would had been led to the recited drain region size through routine experimentation within the teachings of the process of Jin et al. and Odake et al. to achieve a desired property of the transistor device

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. ('665 B1) in view of Odake et al. ('869) as applied to claims 1-6 above, and further in view o0f Ishimaru et al. (U.S. 6,365,472 B1).

The combined teachings of Jin et al. and Odake et al. substantially teach all aspects of the invention but fail to teach wherein the spacers are formed of a layer of

silicon nitride on which a layer of polycrystalline silicon is deposited. However, Ishimaru et al. in a related method to form a transistor device teach forming a first spacer (6) over the sidewalls of a gate electrode (3); and forming a layer of polycrystalline silicon (7) over the silicon nitride sidewall (6) (column 4, line 58 – column 5, line 16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ishimaru et al. in the transistor device of Jin et al. and Odake et al. to enable the formation of the polycrystalline silicon layer over the silicon nitride spacer as taught by Ishimaru et al., and furthermore to protect the substrate from implantation steps, thus reducing damages to the underlying substrate and reducing current leakage (column 2, lines 42 – 50).

Response to Arguments

6. Applicant's arguments filed 7/12/2003 have been fully considered but they are not persuasive.

Applicant argues, "...Jin, Odake, and Fulford, either separately or in combination, fail to teach or suggest the claimed invention...a gate oxide layer is formed on a surface of a semiconductor body of silicon, on which a gate oxide layer the gate electrode containing a polycrystalline silicon layer is provided locally. As the Office indicated in the Office Action, Jin fails to teach this...". In response to this argument, Jin et al. teach in Fig.4B, for example, "a gate oxide layer formed on a surface of a semiconductor body of silicon, on which a gate oxide layer the gate electrode containing a polycrystalline silicon layer is provided locally" as argued. Also, contrary to applicants' latter argument,

the Office didn't indicated in the office action that Jin et al. fail to teach the above-mentioned argument.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-

mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
9/22/03

George Fourson
Primary Examiner